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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,731	10/23/2000	Barrie Gilbert	1482-138	3741

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/694,731	GILBERT, BARRIE	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-12, 14, 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 1/8/2002. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hofmann (USP 4250457).

As to claims 1 and 8, Hofmann discloses in figure 2 a transistor cell, and method thereof, comprising: an input terminal (node between 38 and 16) for receiving an input signal, an output terminal (node between 14 and 16) for transmitting an output signal, a grounded base transistor (16) coupled between the input and output terminals, and a current mirror (32, 38) coupled between the input and output terminals, the method comprising biasing the transistor cell (40, 42) to establish a bias current in the grounded base transistor and the current mirror when the input signal is zero; and limiting the input signal to a range in which the output function of the transistor cell approximates a square-law (figure 3 and column5, lines 15-18), as further called for claim 8, figure 2 shows the bias signal generator generates a bias signal that varies with temperature such that it causes the bias current through each of the transistors to be proportional to absolute temperature.

As to claim 3, figure 2 teaches adjusting the bias current (by temperature), thereby adjusting the input impedance cell.

As to claim 4, figure 2 teaches the bias transistor cell includes: coupling a bias signal (signal at node between 26 and 28) to the base of the grounded transistor; and varying the bias signal with temperature such that it causes the bias current through the grounded base transistor and the current mirror to be proportional to absolute temperature.

As to claim 5, figure 2 shows the current mirror is coupled to a power supply terminal (ground); and biasing the transistor cell includes maintaining the base of the grounded base transistor at about 2VBE from the voltage of the power supply terminal.

As to claim 6, figure 2 teaches isolating the current mirror from the output terminal (by transistor 16 and 43).

As to claim 7, figure 2 teaches isolating the current mirror includes coupling a cascode transistor (43) between the output terminal and the current mirror.

As to claim 9, figure 2 shows a cascode transistor (43) coupled between the current mirror and the output terminal.

As to claim 10, figure 2 shows the current mirror is coupled to a power supply terminal (ground), and the bias signal generator (28, 30) maintains the base of the grounded base transistor at about 2VBE from the voltage of the power supply terminal.

As to claim 11, figure 2 shows the current mirror includes: a diode connected transistor (38) coupled between the input terminal and a power supply terminal (ground); and a mirror transistor (32) having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

As to claim 12, figure 2 shows the grounded base transistor has a collector coupled to the output terminal, a base for receiving the bias signal, and an emitter coupled to the input terminal; a current mirror includes: a diode-connected transistor (38) having a collector and base coupled to the input terminal and an emitter coupled to a power supply terminal, and a mirror transistor (32) having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

As to claim 14, figure 2 shows the bias signal generator includes: two diode-connected transistors (40, 42) coupled in series between the input terminal and power supply terminal; and a current source (26) coupled to the diode connected transistors to cause a bias current to flow through the diode connected transistors.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann (USP 4250457).

Figure 2 shows all limitations of the claim except for the step of limiting the input signal to less than about four times the bias current. However, figure 3 shows the input current can be smaller than the bias current. Therefore, the selection for the input signal to be less than about four times the bias current is seen as an obvious design choice dependent upon particular environment of use to ensure optimum, performance.

Response to Arguments

5. Applicant's arguments have been fully considered but they are not persuasive.

Applicant states that Hofmann fails to shows the step of limiting the input signal to a range in which to output function of the transistor cell approximates a square-law. The Examiner respectfully disagrees. Figure 2 and the equation in column 5, lines 15-18, show the output function of the transistor cell approximates a square-law.

With respective to the argument of claims 4 and 8, the phase "such that" is a result. Hofmann's figures 1 and 2 having similar structure with Applicant's figure 1. Therefore, the current going through each of transistor is proportional to absolute temperature is seen as a result in Hofmann's circuits.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
March 4, 2002

Terry D. Cunningham
Primary Examiner